REMARKS

Claims 1-25 will be pending upon entry of the present amendment. Claims 16-25 are new.

The Examiner objected to the declaration because it does not include the address of each inventor. The applicants respectfully disagree. As indicated on page 2 of the Office Action and in 37 CFR § 1.63(c), the mailing address may be properly supplied in an Application Data Sheet (ADS). In the ADS filed with the application on October 2, 2003, the mailing address of each inventor is listed. As such, the declaration properly does not include the mailing address of each inventor.

The abstract of the disclosure was objected to for exceeding 150 words. A revised abstract is being supplied which includes only 150 words.

The disclosure was objected to for failing to include a sentence starting with "I (or we) claim" or the like. The specification is being amended to include the suggested language.

The numbering of the original claims was objected to because two claims were numbered 14. The applicants appreciate the Examiner's amendment renumbering the second claim 14 as claim 15.

Claims 1-4, 6-7, and 10-12 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,696,698 to Herluison et al. ("Herluison") in view of U.S. Patent Publication Nos. US20010050955A1 to Zhang et al. ("Zhang") and US20020101536A1 to Cook et al. ("Cook").

The cited prior art does not teach or suggest the invention recited in claim 1. Claim 1 recites a cache memory system that is structured in one of two arrangements:

> a first arrangement having banks of memory from the second cache memory concatenated vertically such that their concatenated height is at least equal to a first height of the first cache memory, and said concatenated banks being arranged to be appended to the width of the first cache memory to form a single contiguous address space, and
>
> a second arrangement having banks of memory from the first and second caches stacked vertically, and arranged to be addressed as two separate address spaces.

The cited prior art does not teach either of the two arrangements recited in claim 1, including cache banks stacked or concatenated vertically. Herluison shows a first cache memory 1 with segments arranged horizontally next to one other and a second cache memory 2 not disclosed as having any banks or any arrangement with respect to the first cache memory 1. Thus, Herluison does not suggest "banks of memory from the second cache concatenated vertically," "said concatenated banks being arranged to be appended to the width of the first cache memory to form a single contiguous address space," or "banks of memory from the first and second caches stacked vertically."

The Examiner incorrectly asserts that Herluison describes banks of memory from the first and second caches being stack vertically, citing column 4, lines 45-49. First, Herluison never mentions or shows any banks of the second cache 2. Second, the referenced lines of column 4 refer to sequential motions of a picture in horizontal and vertical directions rather than any relationship between banks of cache memory. Nothing in Herluison suggests that banks of cache memory are arranged according to the pixels of the picture being analyzed. Nothing in motion estimation would suggest or require a cache memory to be rotated 90° in order to perform motion estimation in the vertical direction.

Zhang and Cook do not teach or suggest the vertical stacking or concatenation that is missing from Herluison. Zhang does not show or even mention any memory banks of a cache memory, and thus, cannot suggest vertical stacking or concatenating of such memory banks. Instead, Zhang discusses vertical "slits," which are vertical image rays of a camera (0075), that form macroblock groups (MPG) that can be accessed and decoded together (0077). Like Herluison, there is nothing in Zhang suggesting that the vertical slits or MPGs of Zhang are stored in cache memory banks that are stacked or concatenated vertically. The Examiner points to paragraph 0131 of Zhang, but paragraph 0131 merely mentions that there are four different caches 402-408' without suggesting that the caches or memory banks of the caches are stacked or concatenated vertically. Moreover, the Examiner asserts that paragraph 0077 of Zhang indicates that vertical stacking improves speed, but paragraph 0077 does not state or imply anything of that sort. Instead, paragraph 0077 states that in using redundant slits, speed will be acceptable due to the use of cache memory, without suggesting anything regarding the arrangement of the cache memory.

Cook does not remedy the inadequacies of Herluison and Zhang. Cook shows nothing more than a single contiguous memory space with Y data store in the top portion and U and V data stored in the bottom portion in Figure 3B. As indicated in paragraph 0010, Figure 3B shows color space data, not memory banks of a cache memory. In fact, the only mention of a cache in Cook appears to be claim 11, which does not state or imply that the cache even includes plural memory banks, let alone vertically stacked memory banks.

In summary, the Examiner's assertion of obviousness appears to be based almost entirely on a confusion between relative locations of pixels or block within an image and relative arrangements of cache memory banks. There is nothing in the cited prior art suggesting that cache memory banks are arranged according to relative pixel or block locations within images. In other words, just because one image block is located above another image block, that does not mean that the image blocks are respectively stored in cache memory banks that are concatenated or stacked vertically. Zhang and Cook simply do not even mention any cache memory banks and Herluison only shows segments s1-s4 of one cache memory 1 being arranged horizontally. Such teaching cannot suggest the vertical stacking or concatenation recited in claim 1.

For the foregoing reasons, claims 1-4 are nonobvious in view of the cited prior art.

Although the language of claims 6-7 and 10-12 is not identical to that of claim 1, the nonobviousness of claims 6-7 and 10-12 will be apparent in view of the above discussion.

Claims 5, 13, and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over Herluison, Zhang, and Cook in view of U.S. Patent No. 5,535,288 to Chen et al. ("Chen").

The cited prior art does not teach or suggest the invention recited in claims 5 (dependent on claim 1) and 13-14 (dependent on claim 10) because Chen does not teach or suggest the features of claims 1 and 10 that are missing from Herluison, Zhang, and Cook. Chen does not even appear to mention a cache memory or plural memory banks, and thus, cannot suggest vertical stacking or concatenation of cache memory banks. Accordingly, claims 5 and 13-14 are nonobvious in view of the cited prior art.

Claim 8 was rejected under 35 U.S.C. § 103 as being unpatentable over Herluison, Zhang, and Cook in view of U.S. Patent No. 5,510,857 to Kopet et al. ("Kopet").

The cited prior art does not teach or suggest the invention recited in claim 8 (dependent on claim 6) because Kopet does not teach or suggest the features of claim 6 that are missing from Herluison, Zhang, and Cook. Kopet shows in Figure 1 a local memory 54, but does not suggest that the local memory 54 has plural memory banks, and thus, cannot suggest vertical stacking or concatenation of cache memory banks. Accordingly, claim 8 is nonobvious in view of the cited prior art.

Claim 9 was rejected under 35 U.S.C. § 103 as being unpatentable over Herluison, Zhang, and Cook in view of U.S. Patent No. 6,567,091 to Dye et al. ("Dye").

The cited prior art does not teach or suggest the invention recited in claim 9 (dependent on claim 6) because Dye does not teach or suggest the features of claim 6 that are missing from Herluison, Zhang, and Cook. Dye shows in Figures 33 and 35 a cache memories 838, 810, but does not suggest that either of the cache memories 838, 810 has plural memory banks, and thus, cannot suggest vertical stacking or concatenation of cache memory banks. Accordingly, claim 9 is nonobvious in view of the cited prior art.

Claim 15 was rejected under 35 U.S.C. § 103 as being unpatentable over Herluison, Zhang, and Cook in view of U.S. Patent No. 5,995,668 to Corset et al. ("Corset").

The cited prior art does not teach or suggest the invention recited in claim 15 (dependent on claim 10) because Corset does not teach or suggest the features of claims 1 and 10 that are missing from Herluison, Zhang, and Cook. Corset does not even appear to mention a cache memory or plural memory banks, and thus, cannot suggest vertical stacking or concatenation of cache memory banks. Accordingly, claim 15 is nonobvious in view of the cited prior art.

New claims 16-17 depend on claim 1, and thus, a nonobvious in view of the cited prior art for the reasons expressed above. In addition, claims 16-17 recite further features that are not taught or suggested by the cited prior art. Claim 16 recites that, in the second arrangement, each bank of the first cache memory is stacked with a corresponding one of the banks of the second cache memory, thereby forming a set of logical banks that each include one bank of the first cache memory and the corresponding bank of the second cache memory. Claim 17 further adds that a first address space includes first portions of each of the banks of the first cache memory and a second address space including the banks of the second cache memory and second portions of each of the banks of the first cache memory. Nothing in the cited references suggests such stack cache memory banks, logical banks, or first and second memory spaces that include respective portions of the banks of a first cache memory. Accordingly, claims 16-17 are in condition for allowance.

Although the language of new claims 18-19 is not identical to that of new claims 16-17, the allowability of claims 18-19 will be apparent in view of the above discussion.

New claims 20-21 are directed to an embodiment like the first arrangement of claim 1 while new claims 22-25 are directed to an embodiment like the second arrangement of claim 1. Thus, the allowability of claims 20-25 will be apparent in view of the above discussion.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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